

CXL 2.0 Use Case

Using Both DDR4 & DDR5 on the Same Server to Allow Memory & Bandwidth Scaling

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**MEMORY FABRIC
FORUM**



**OCP
GLOBAL
SUMMIT**

OCT 15-17, 2024
SAN JOSE, CA

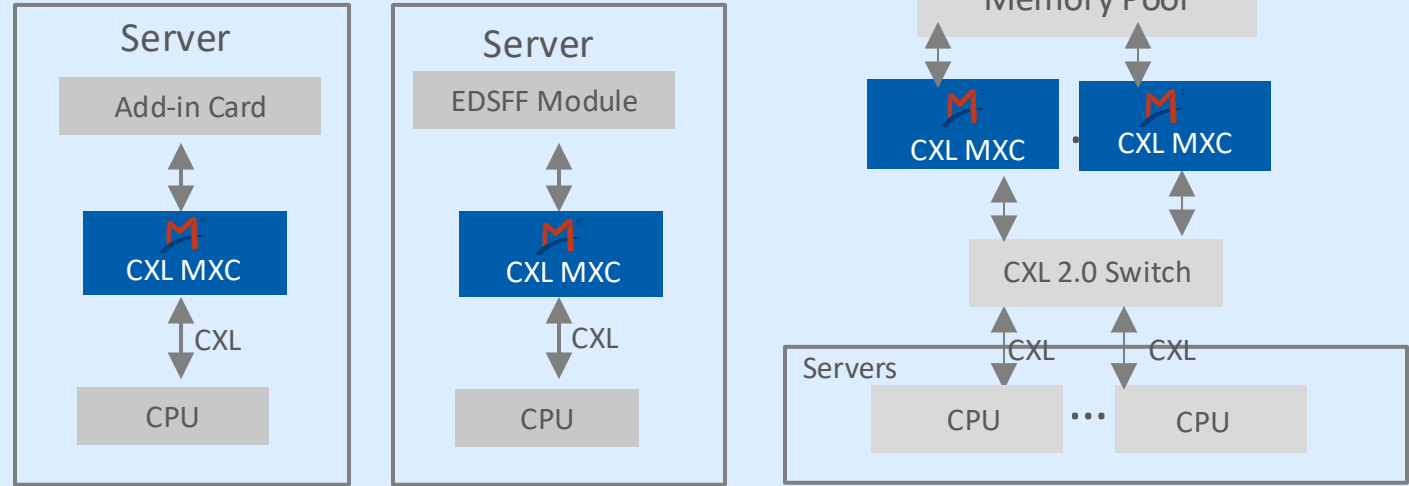


About Montage Technology

- More than 20 years in memory products - leading the industry on DDR4 and DDR5 memory interface products
- PCIe Gen 4 and 5 Retimer portfolio with design wins around the world
- Leading in shipments and mass production of CXL controllers
- World Wide ecosystem enabling in cloud computing & data center markets

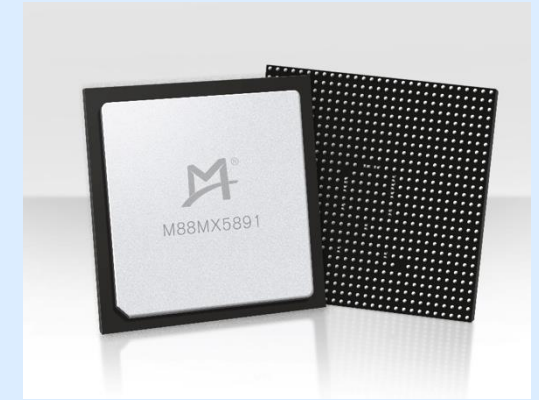
CXL technology-based solutions available today and future products in the pipeline!

CXL Adoption in the Datacenter



Memory Expansion

Memory Pooling

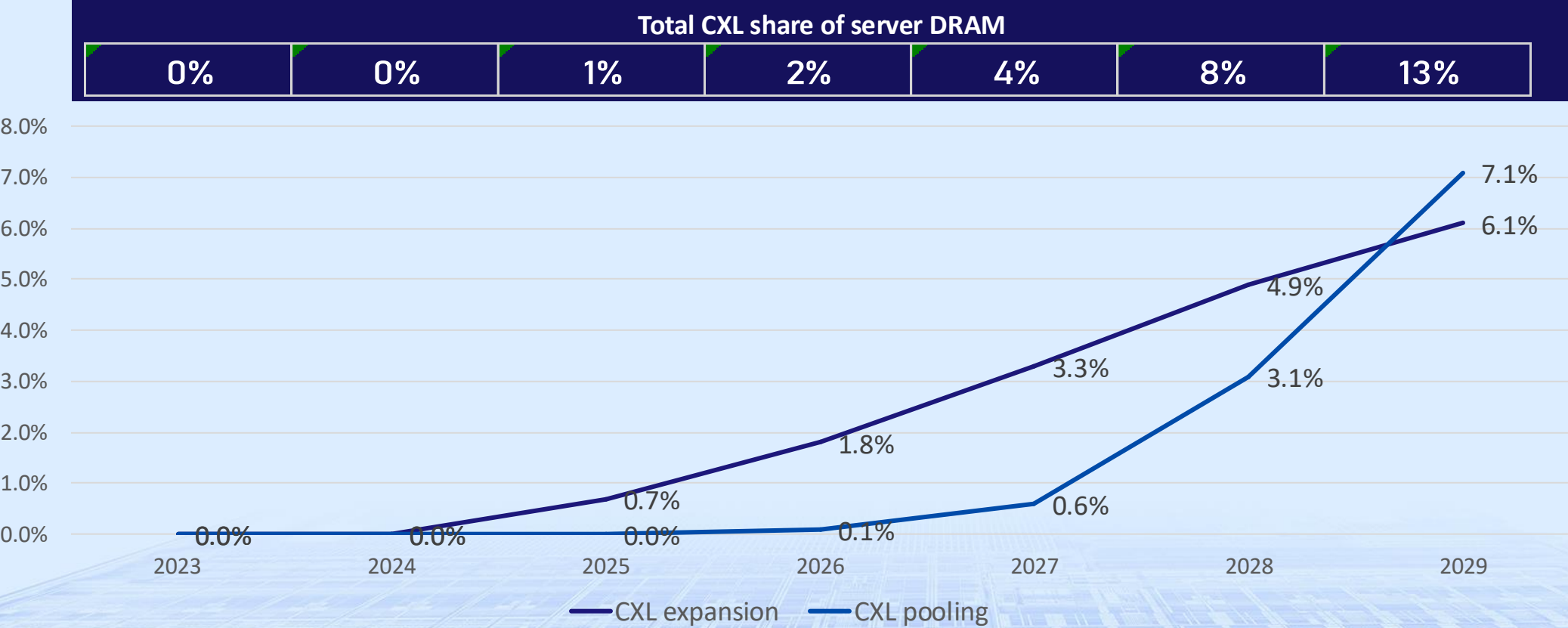


- Industry's leading Type 3 CXL Memory eXpander Controller (MXC)
- Providing high-bandwidth and low-latency interconnect between CPU and CXL-based devices to enable memory expansion and pooling for data centers
- Compliant with DDR4/DDR5 JEDEC and CXL 2.0 specifications, supporting PCIe 5.0 speeds
- Designed for use in Add-In Card (AIC), EDSFF Memory Module and CXL pooled memory

CXL Share of Server Bit Demand

DRAM behind CXL will grow to ~10% of server DRAM by 2029.

Share of server bit demand*



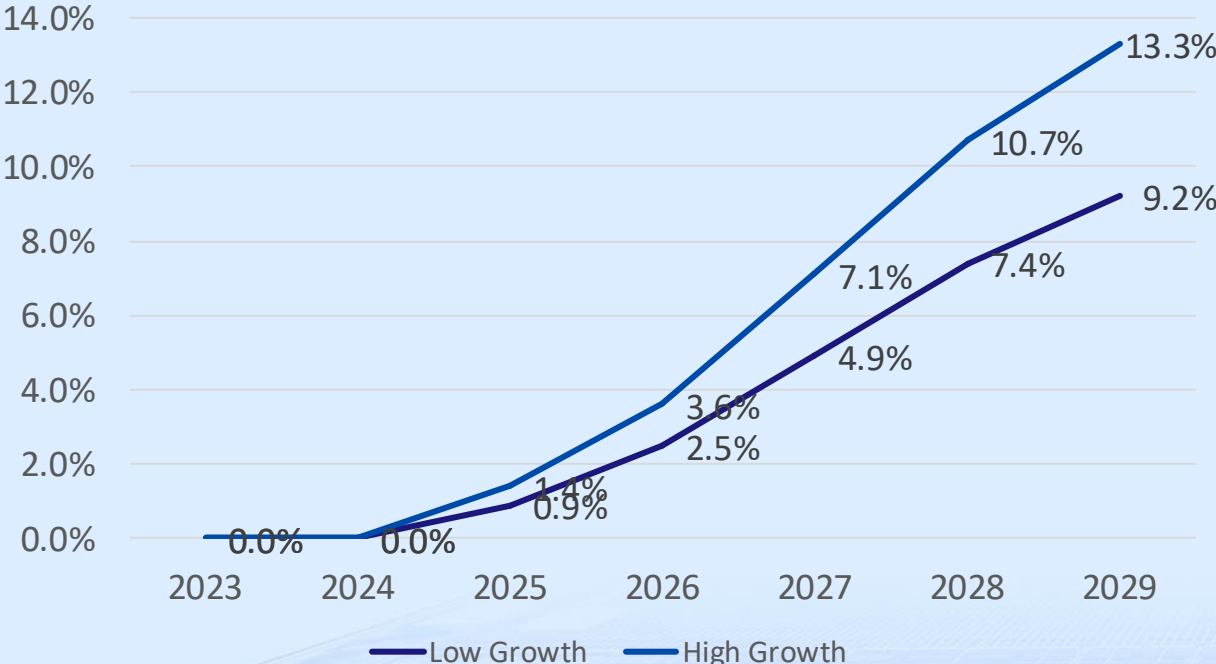
* Excludes GDDR and HBM

Source: Tech Insights Aug '24

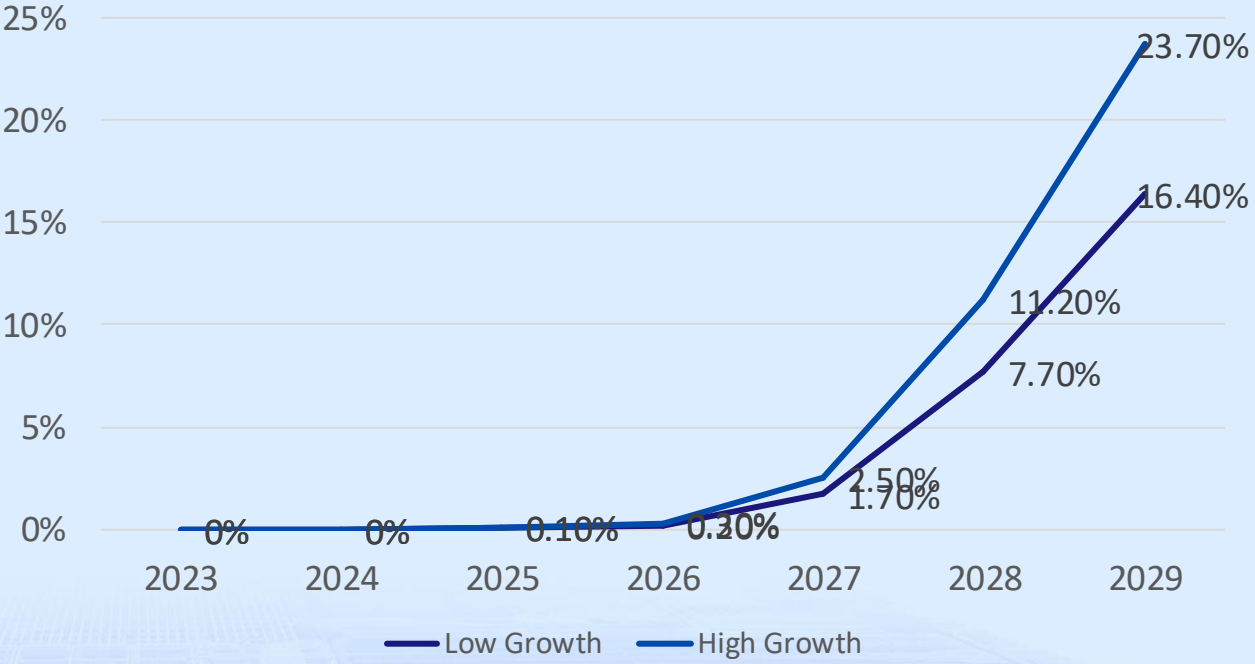
CXL Adoption in the Datacenter – Two Areas of Opportunity

Expansion usage is being challenged by 32Gb monolithic die (and corresponding 128GB RDIMM) & the emergence of MRDIMM (with higher bandwidth).

CXL Expansion Adoption (% of servers using CXL)



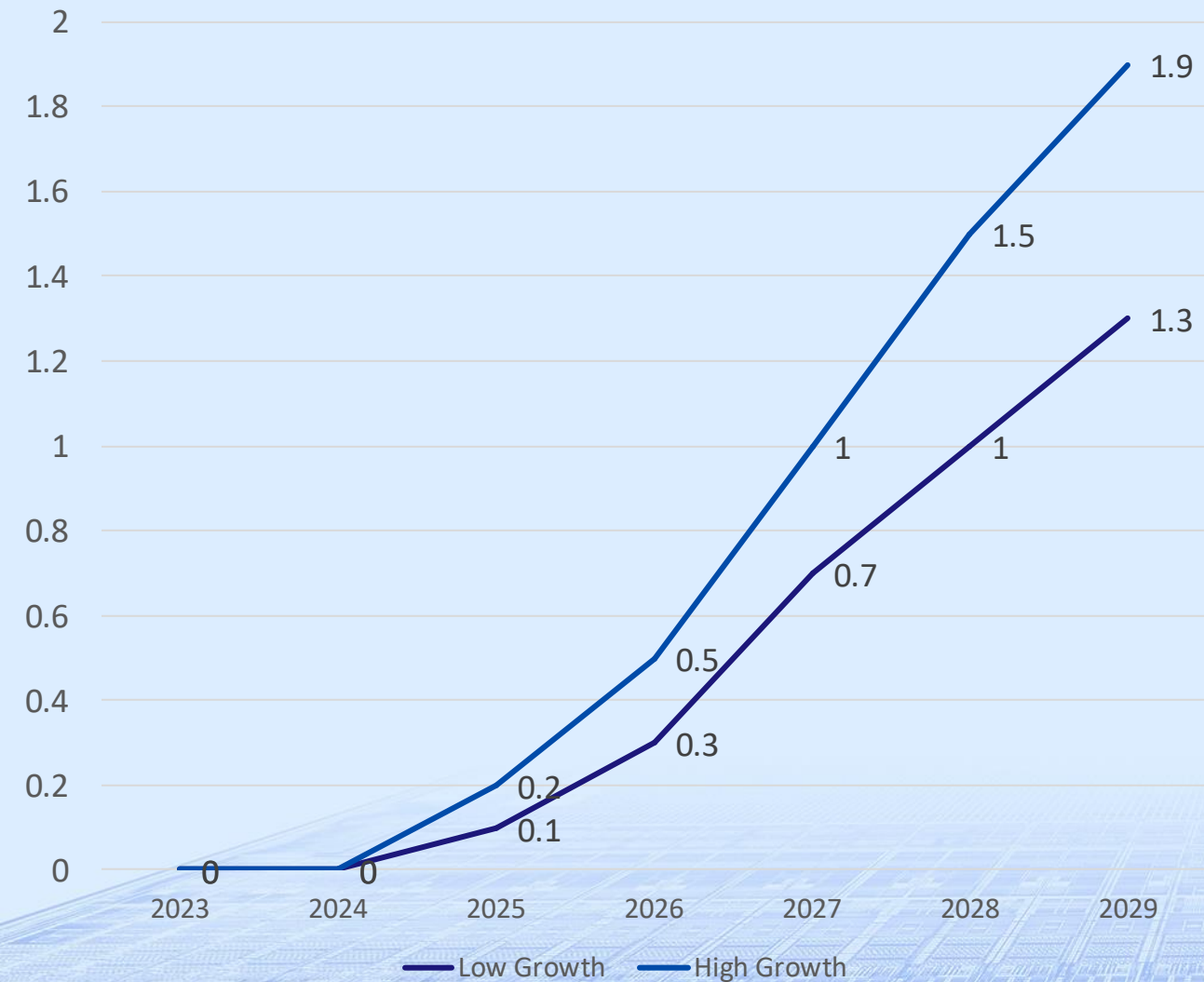
CXL Pooling Adoption (% of servers using CXL)



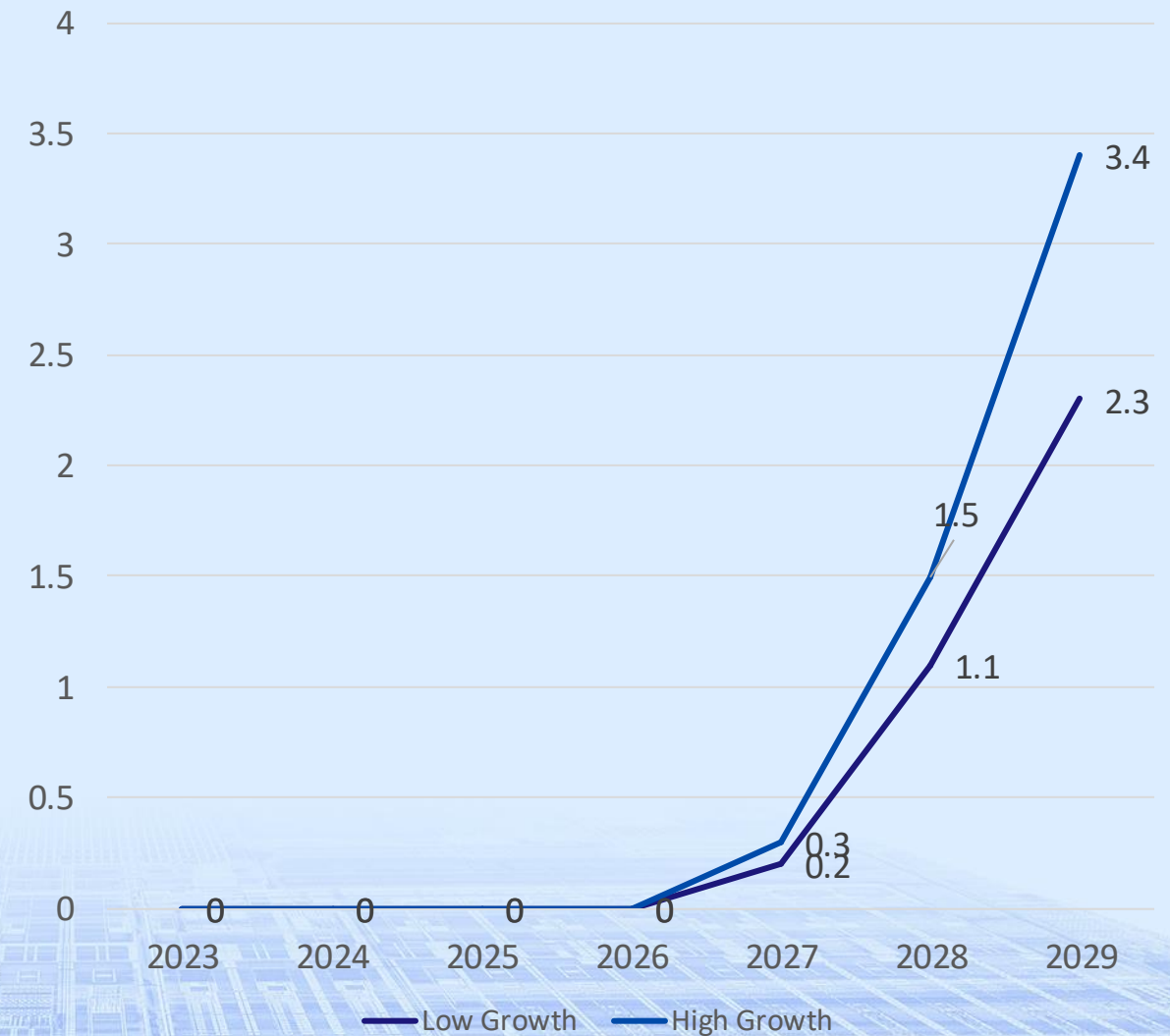
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CXL adoption in the datacenter - units

CXL Expansion Units (million)



CXL Pooling Units (million)



CXL Memory eXpander Controller: MXC

M88MX5891 MXC GEN1 Product:

- CXL Type 3 Memory Expander
- CXL 1.1/2.0 compliant
- DDR4-3200 up to 2DPC
- DDR5-5600 1DPC and DDR5-4800 2DPC
- Rich RAS features
- Security Features
- Support E3.s without using RCD
- Ultra Low Power

M88MX5851 MXC GEN2 Product addition:

- Support DDR5 only
- DDR5-6400 and DDR5-5600 2DPC
- 100ns Pin to Pin Latency
- Meta Data Storage
- CXL.IO & CXL.MEM IDE
- Montage DDR Characterization Features



DRAM Bandwidth and Capacity Aggregation across Multiple CXL™ Modules

CXL DRAM Memory Controller (MXC)

- CXL Type3 Memory Expander
- CXL 1.1 / 2.0 Compatible
- CXL.IO Gen5 support, up to 32GT/s
- Fully JEDEC DDR4/5 complaint and capable
- Rich RAS features supported
- DDR4 up to 3200 MT/s and DDR5 up to 6400 MT/s
- High BW utilization & efficiency
- Single Numa Hop Memory Latency optimized
- Ultra-Low Power Design optimized for Modules

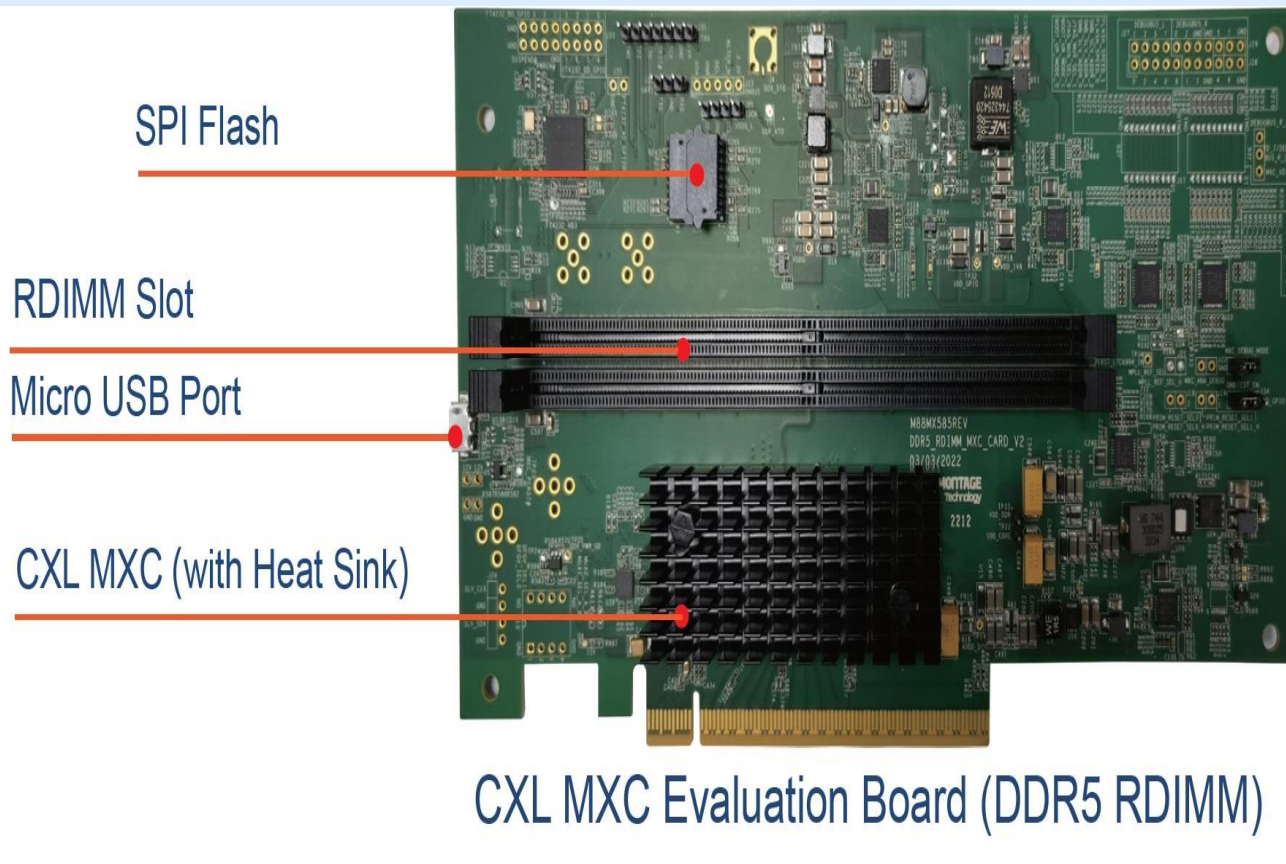
Partners:

MemVerge MONTAGE Technology SAMSUNG SK hynix Micron

CXL MXC

MXC Features

The MXC provides *high-bandwidth and low-latency interconnect* between the CPU and the CXL-based devices, allowing them to share memory for higher performance, reduced software stack complexity, and lower data center TCO.



- CXL Type 3 Memory eXpander Controller
 - Integrated x8 CXL Controller
 - 1 Channel DDR 4-3200/DDR5-5600 Controller (GEN1)
 - 1 Channel DDR5-6400 Controller (GEN2)
 - RISC-V micro-processor
 - On-Chip PVT Sensor
 - SMBus, I3C, I2C, SPI, JTAG, UART
 - Integrated RCD for E1/E3 application
 - Rich RAS Feature:
 - Advanced ECC to correct x4 DRAM device
 - Support Meta Data & poison bit
 - hPPR & sPPR
 - Others
 - 19mmX19mm FCCSP package with 0.7mm pitch
- Security
 - Secure Boot
 - Device Authentication & Attestation
 - DICE
 - Secure FW
- Management
 - Support PLDM, SPDM, CCI over MCTP
 - Supports MCTP binding to SMBus, VDM, I3C(GEN2)
 - Supports Mailbox

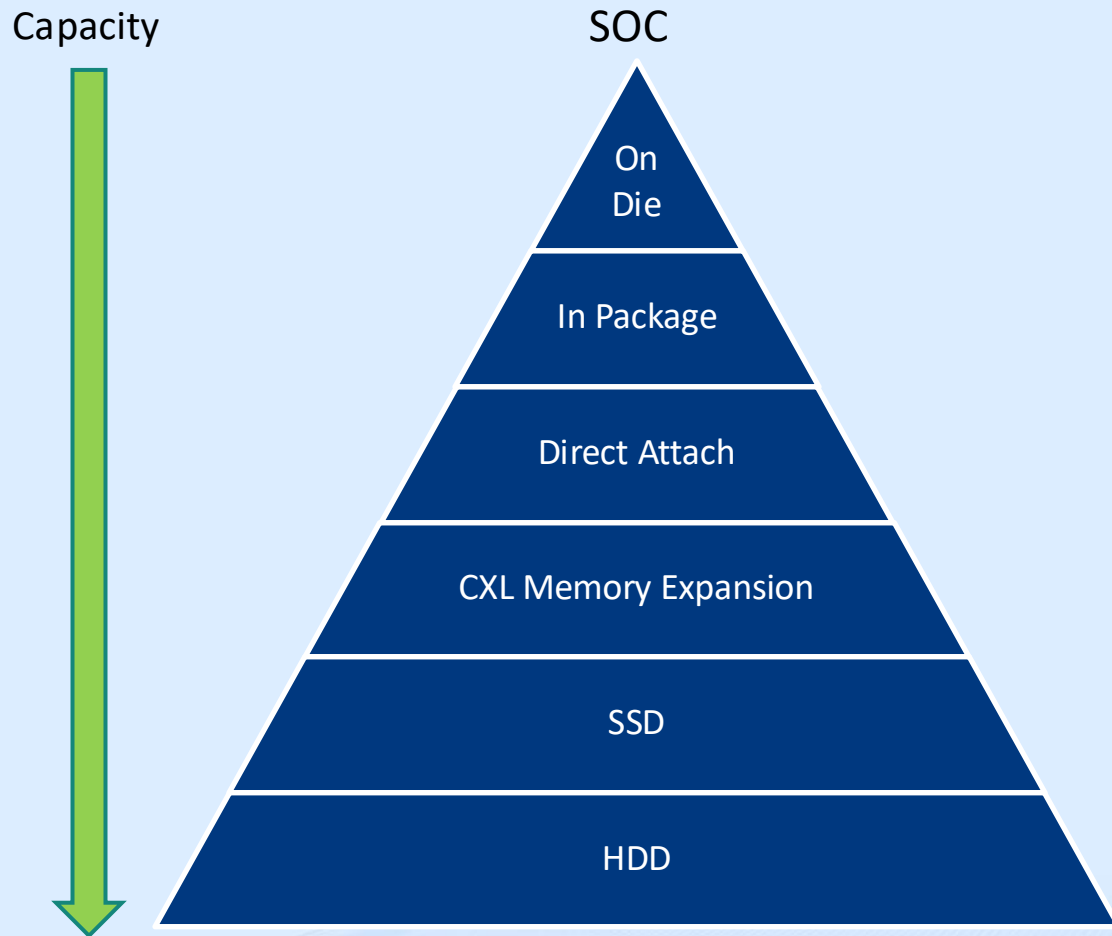


Montage's CXL MXC has been used on Samsung's first 512GB CXL[®] memory module

Montage's CXL[®] MXC has been used on SK hynix's first DDR5 DRAM-based CXL memory module

Note – we have an additional 6 smaller suppliers making AIC and E3 using our controller.

MXC Performance

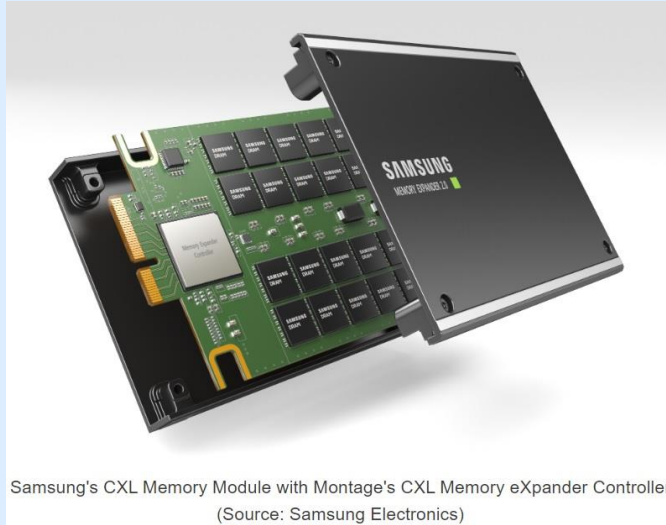


Direct Attach Memory is not able to keep up with the capacity/BW requirements per core.

CXL Memory Expansion addresses this issue!

- 4 ranks DDR5 per sub channel
- Two 40bit DDR5 Sub Channels
- One 72-bit DDR4 channel
- 2 DIMMs per channel
- Accommodate up to 80 DRAM placements
- Low Power
- 1.28TByte Capacity with 3DS DRAM
- Latency Optimized to 1 NUMA hop

MXC Readiness – Components Available Now



Status

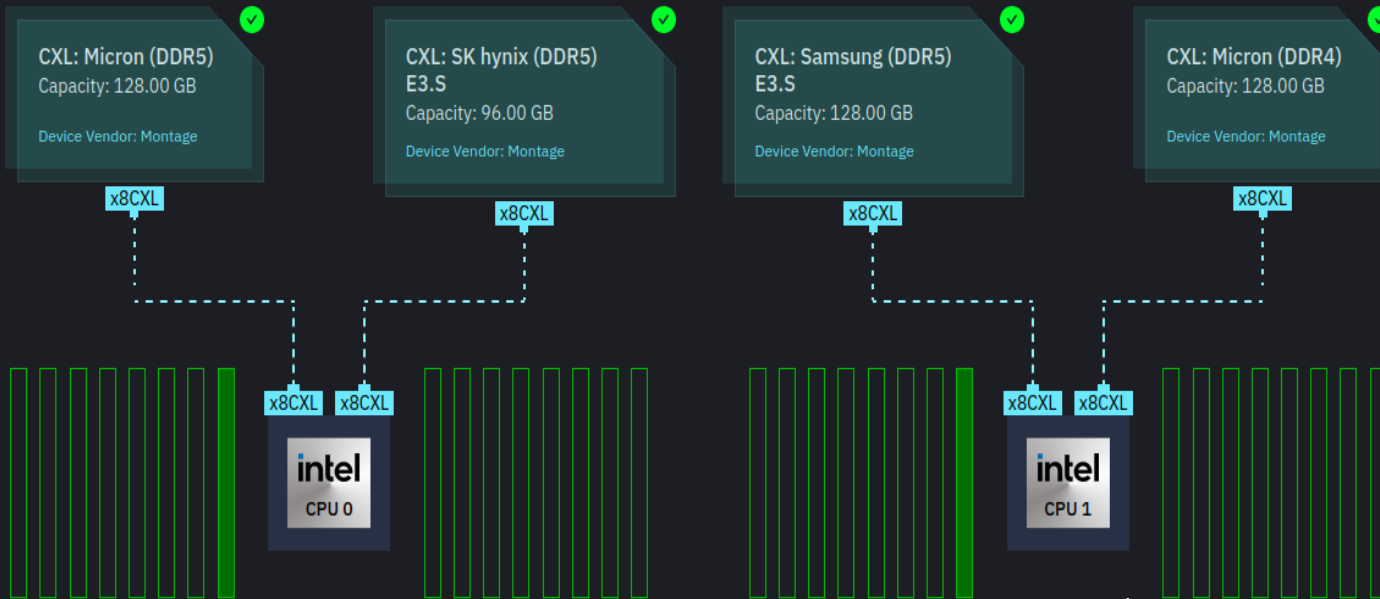
✓ All major SOC suppliers

✓ All major memory suppliers

Contact your module provider for solution availability.



Overview

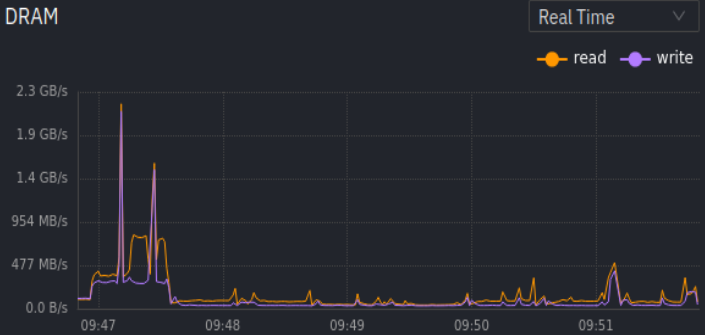


- 17 GB/s Read Write Bandwidth
 - 2 GB/s Read Write Bandwidth

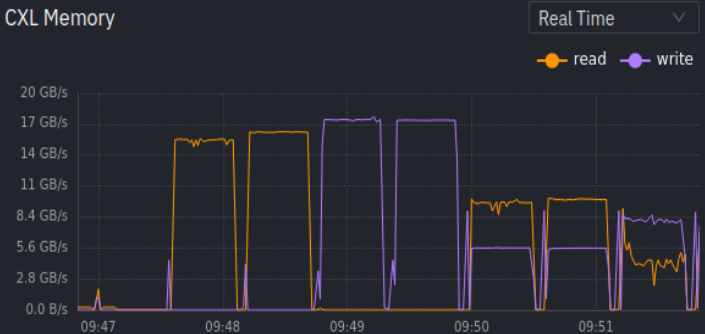
CXL Memory Capacity	480.00 GB
DRAM Capacity	94.10 GB
System Total Capacity	574.10 GB

Usage Throughput CPU

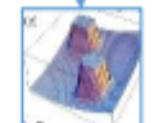
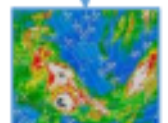
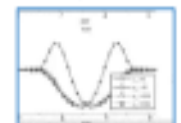
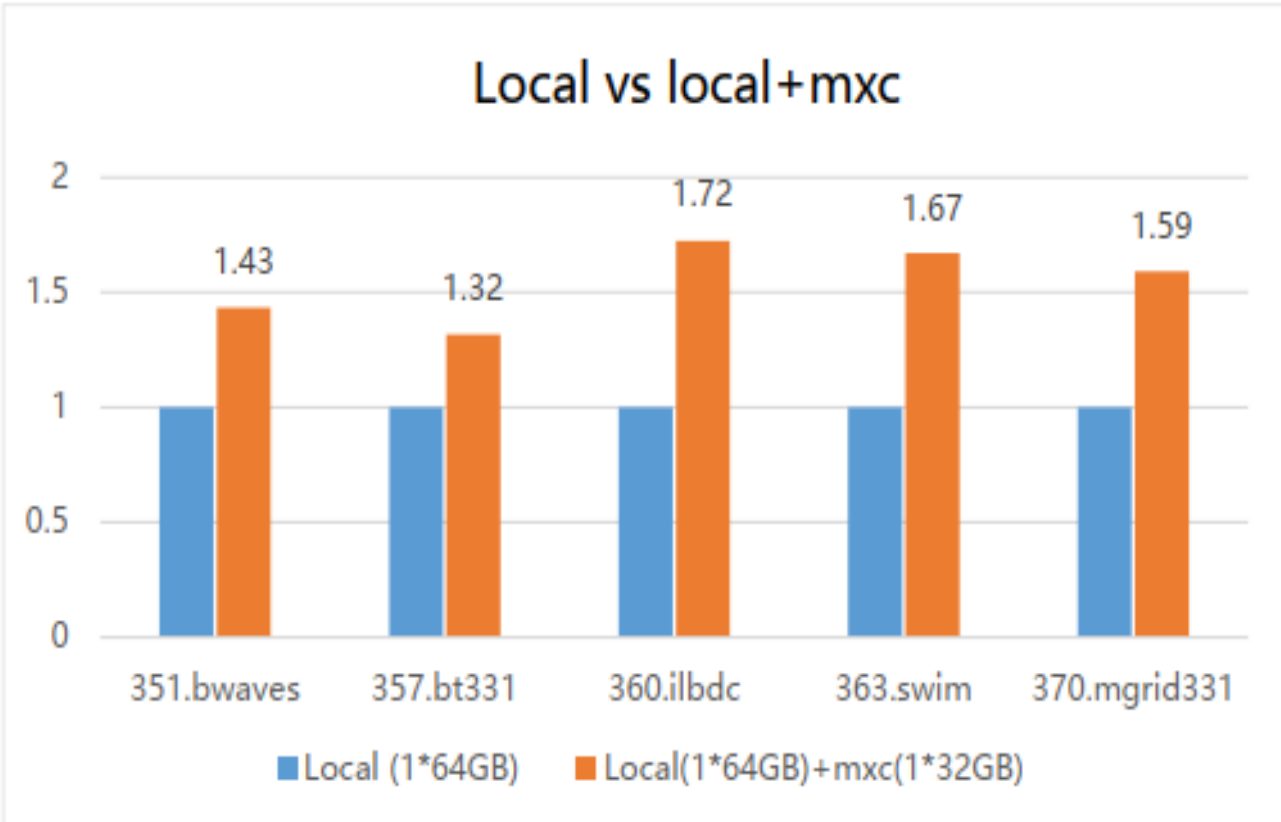
DRAM



CXL Memory



Summary: CXL improves the performance of specific applications in the SPECOMP2012



Platform: Archercity
 CPU: D0 CPU*1
 BIOS: 83D22REL
 DIMM: 64GB Samsung*1
 OS: ubuntu20.4
 Kernel:5:18
 Test cmd: ./app

Local (1*64GB)

Platform: Archercity
 CPU: D0 CPU*1
 BIOS: 83D22REL
 DIMM: 64GB Samsung*1
 OS: ubuntu20.4
 Kernel:5:18
 MXC FW:30R02
 MXC DIMM: Samsung 1Rx4 32GB
 Test cmd: numactl -N 0 -interleave=all ./app

Local (1*64GB) + mxs(1*32GB)

Call to Action

Now is the time to invest in CXL!

The MXC CXL controller is available from Montage today, both as raw silicon and on a reference board.

Add-in card, such as those offered by Samsung & SK hynix, are available today.

Servers with CXL slots are being offered by all major OEMs.

Demonstrations are available showcasing CXL's increases in BW and Capacity performance for memory-bound applications.

[View our demo](#) featuring multiple suppliers with multiple technologies & speeds - all working on Intel and AMD's latest platform.

Thank You

