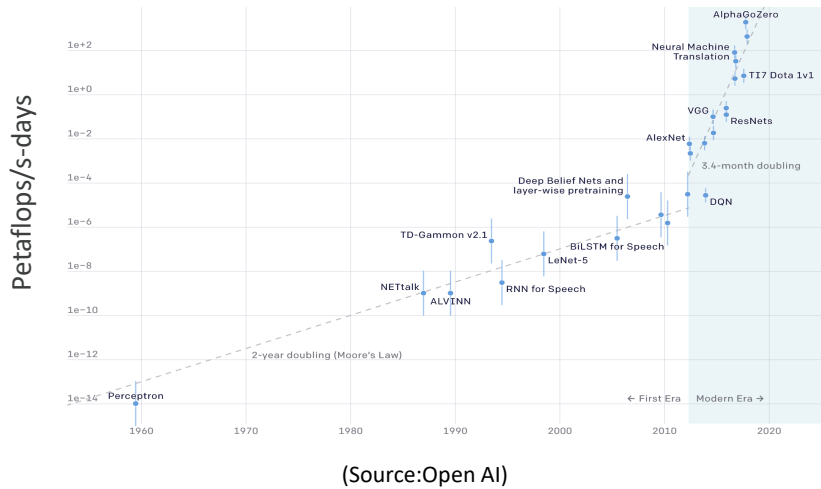# Leo Memory Connectivity Platform

Sandeep Dattaprasad, Senior Product Manager

Flash Memory Summit 2023
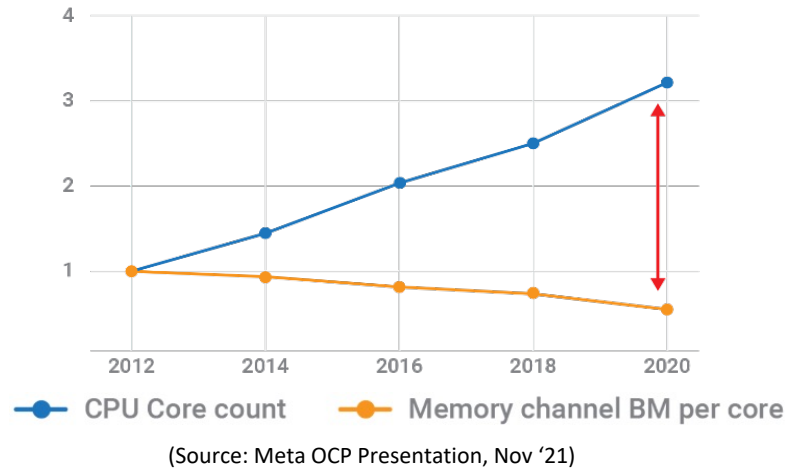
Customer Pain Points in Datacenters

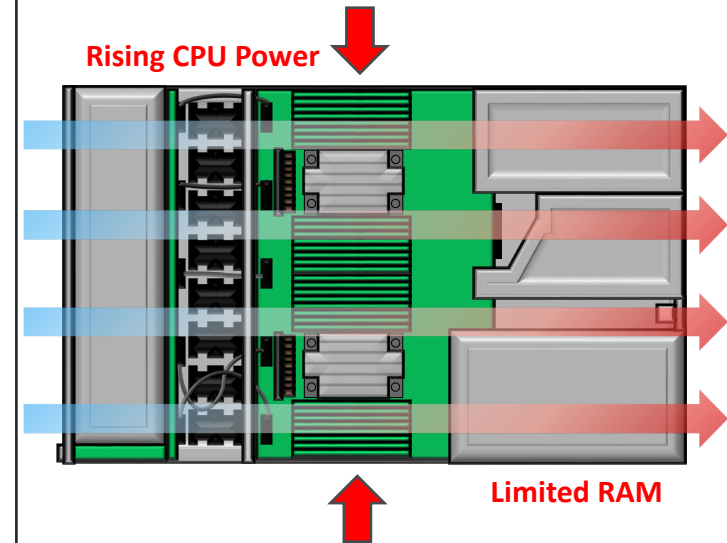## AI/ML Model Complexity and Size
Doubling every 3.5 months

(Source: Open AI)

Computation and Memory Requirements are Outpacing Moore's Law

CPU & Memory Efficiency
Cores vs Memory Bandwidth

CPU Core count   Memory channel BM per core

(Source: Meta OCP Presentation, Nov '21)

CPU & Memory Gap Continues to Widen

Thermal and Mechanical Constraints
32 DIMMs per Server

Rising CPU Power

Limited RAM

Rising TDP (350W) and Data Center Cooling Expenses

Memory Requirements and Bottlenecks Present Challenges at the HW and SW Level

Introducing Leo Memory Connectivity Platform for CXL

Leo Smart Memory Controller

xPU ← CXL 1.1 / CXL 2.0 → CXL 2.0 PHY + Controller | Low Latency Data Path | RAS, Security | CSP Customization | Memory PHY+ Controller ← DDR5 → DIMMs
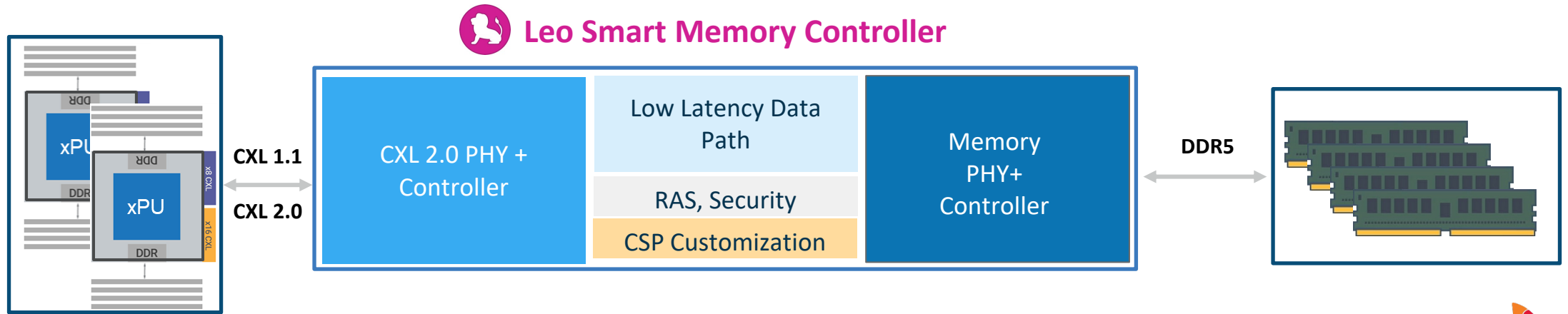
AMD intel arm   SAMSUNG Micron SK hynix

1 Purpose-built for AI/ML workloads in Cloud Servers

2 Server-grade Customizable RAS and Security features.

3 Flexible and Scalable Memory Interface with Low-latency Data Path

4 Seamless Interoperation with Major CPUs/GPUs and Memory DIMMs

AsteraLabs.

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