Meeting Petabyte-scale Memory Systems Challenges with CXL Memory Pooling

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EMPOWERING OPEN.
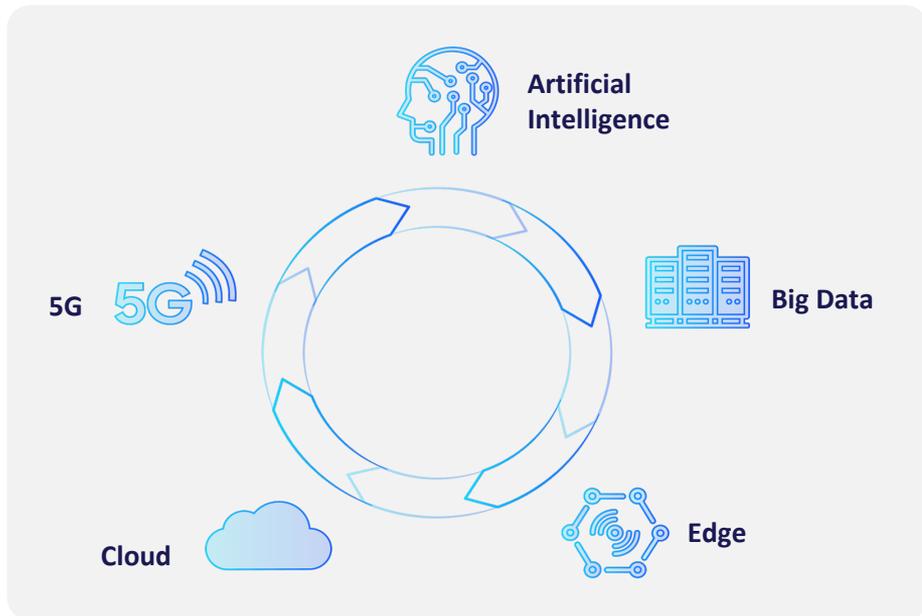
ENDLESS MEMORY
CXL FORUM at OCP Summit

Industry Trends and Challenges

Artificial Intelligence

Big Data

5G

Edge

Cloud

Massive demand for data-centric technologies and applications

Memory bandwidth and density not keeping up with increasing CPU core count

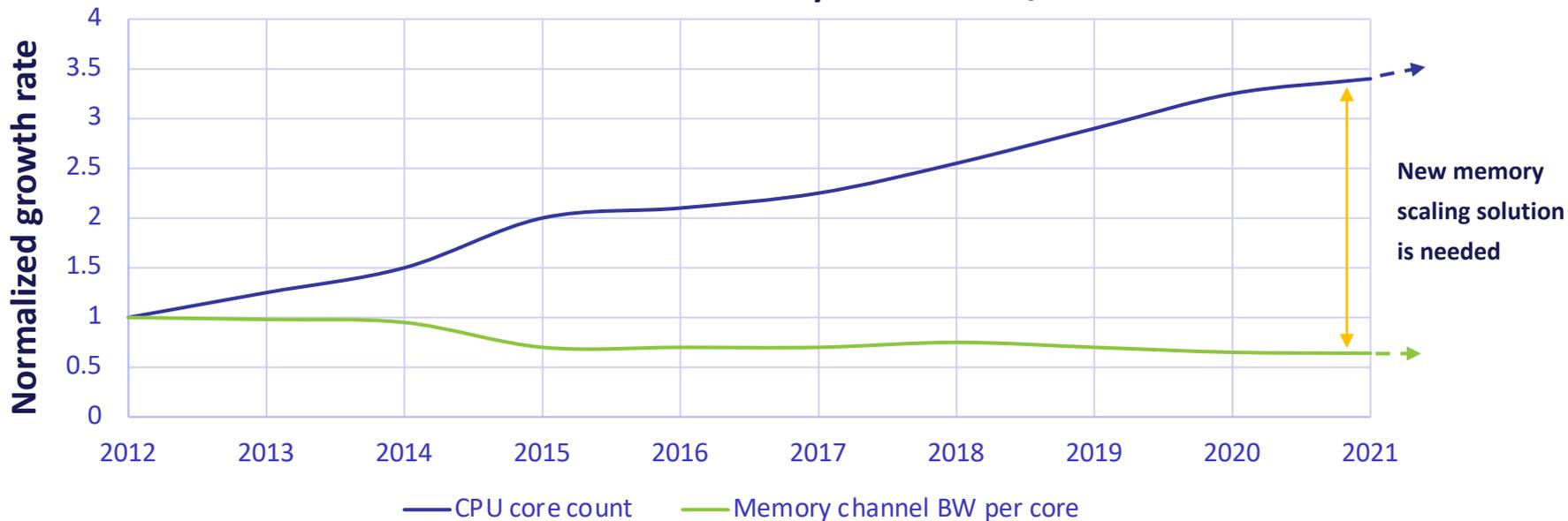**Need a next gen interconnect for heterogeneous computing and server disaggregation**

Industry Trends and Challenges

CPU Core Count vs. Memory Channel BW/core

New memory scaling solution is needed

CPU core count — Memory channel BW per core

Evolution of Hyperscale Computing Environment

- From Converged to Composable architecture
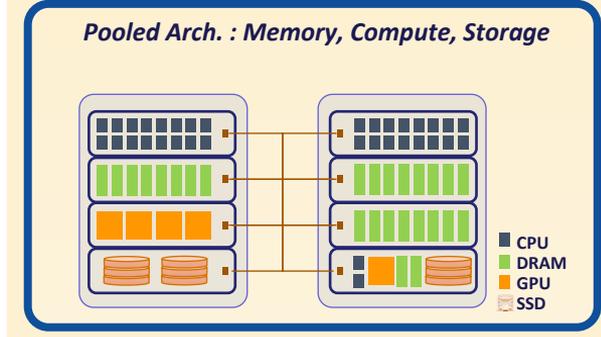
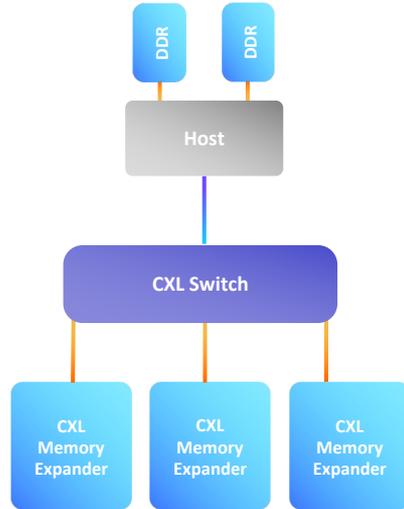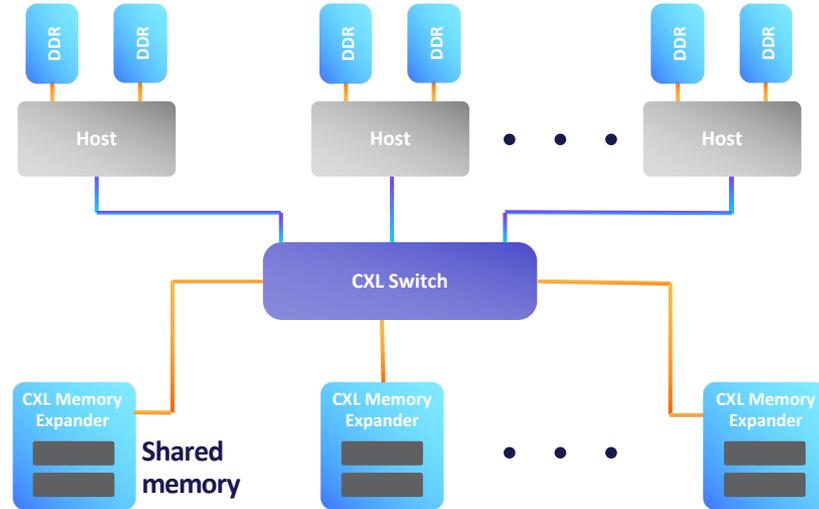# CXL Memory Switching and Pooling – CXL 2.0

- Memory pooling for Type 3 device – Single device can be pooled across 16 virtual hierarchies

Switching to enable memory expansion
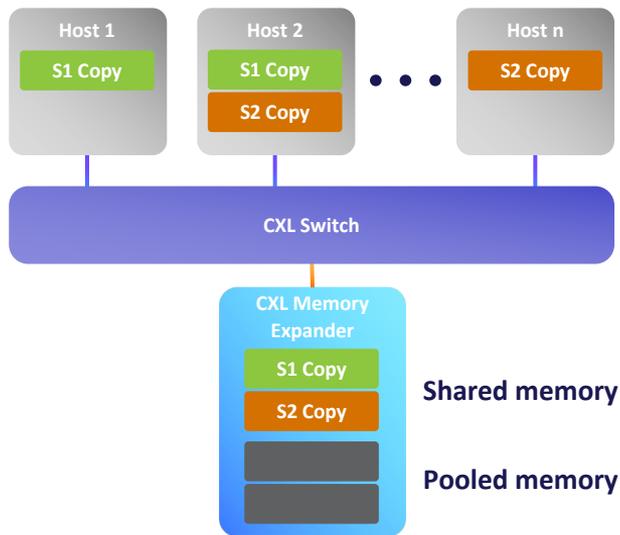
Pooling for increased system efficiency

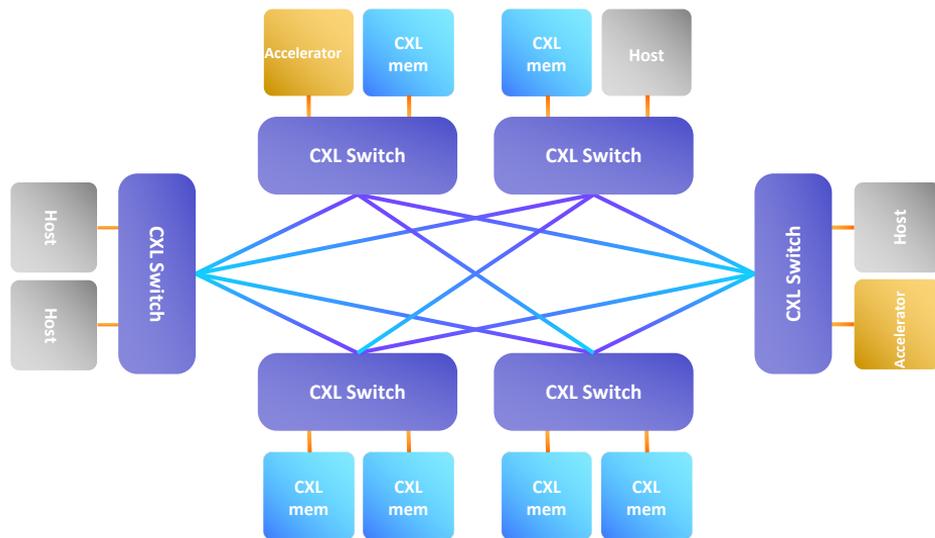# CXL Memory Switching and Sharing – CXL 3.0

- Coherent memory sharing, multi-level switching, and massive scalability with CXL Fabrics

Shared / pooled memory across hosts

Mesh switch topology for highly scalable resources sharing

Samsung Memory Expander (1/2)

- Solution overview
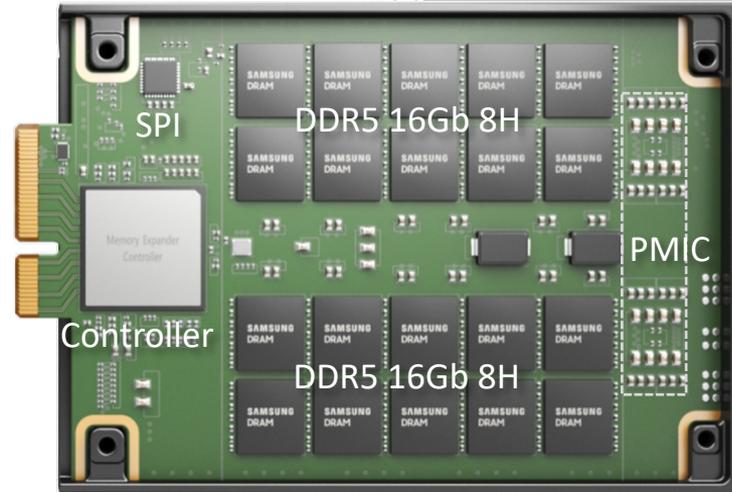
E3.S Form Factor

Samsung Memory Expander (2/2)

- Industry's first ASIC-based CXL memory module – samples already available for evaluation

- Specification – CXL 2.0
- Form Factor - EDSFF (E3.S)
- Media - DDR5
- Module Capacity – up to 512 GB
- CXL Link Width - x8
- Maximum CXL Bandwidth - 32GB/s (PCIe 5.0)
- Other Features - RAS, Interleaving, Diagnostics and more:
  - ✓ Viral and data poisoning
  - ✓ Memory error injection
  - ✓ Multi-symbol ECC
  - ✓ Media scrubbing
  - ✓ Post package repairs (hard/soft)

Scalable Memory Development Kit (SMDK)
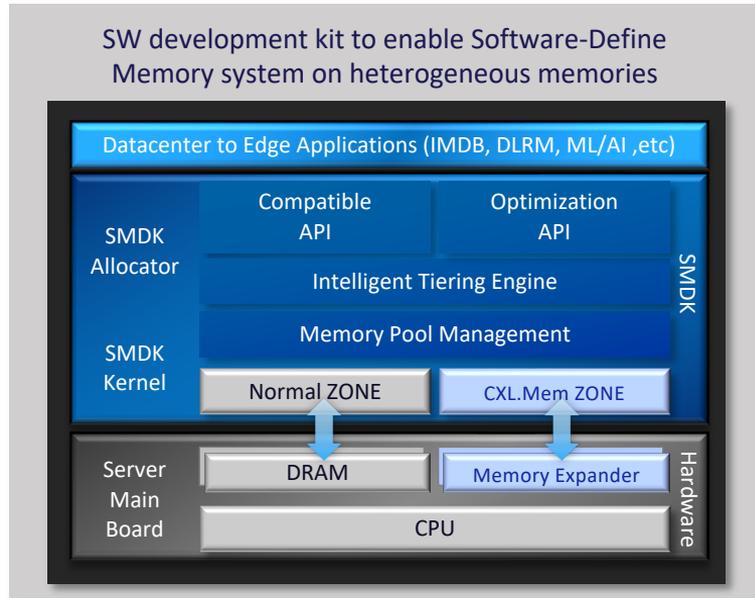
- Unified interface for heterogeneous memory system management

Plug-in

- ➢ **Two selectable paths - Optimization and Compatible Path, with or without modification of application SW**

- ➢ **Intelligent Tiering Engine - supports memory tiering scenarios with prioritiy, capacity, bandwidth, etc.**

- ➢ **Memory Pool Management - supports scalability reflecting memory request status and system resource**

Kernel

- ➢ **Memory Partitioning allows logical memory views for heterogeneous physical DRAM and CXL memory**

Xconn Tech's CXL 2.0 / PCIe5 Switch

- World's first CXL 2.0 and PCIe5 Switch

- ➢ 2,048 GB/s total BW with 256 lanes

- ➢ Lowest port-to-port latency

- ➢ Lowest power consumption per port

- ➢ XC50256 is Xconn Tech's first generation switch
  - TSMC 16nm, T/O in February, 2022

Xconn Tech's CXL 2.0 / PCIe5 Switch Key Features

- Fully compliant with CXL2.0/1.1 and PCIE Gen5

- Support CXL.io, CXL.mem and CXL.cache

- CXL1.1 and CXL2.0 Fabric Manager Interface

- Support MLD (Multiple Logical Device)

- Multiple virtual CXL switches (VCS)

- Support CXL Type2 and Type 3 memory devices

- Total up to 32 ports with Bifurcation

- Full RAS support (ECC/Parity, DPC, Hot-Plug, Data Poisoning)

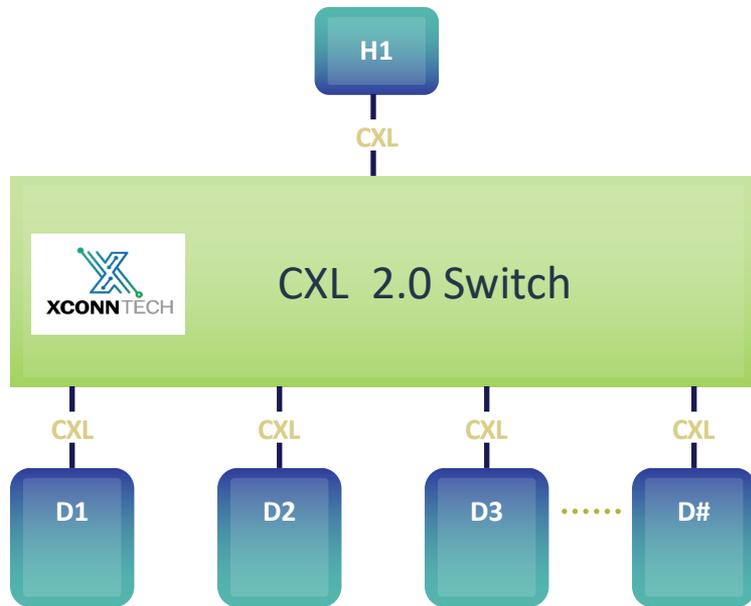# Applications for Memory Expansion

- Xconn CXL 2.0 Switch supports single-level switching to enable fan-out to multiple Type 2/3 devices for memory expansion

- Expand up to 31TB DDR5 with a single switch

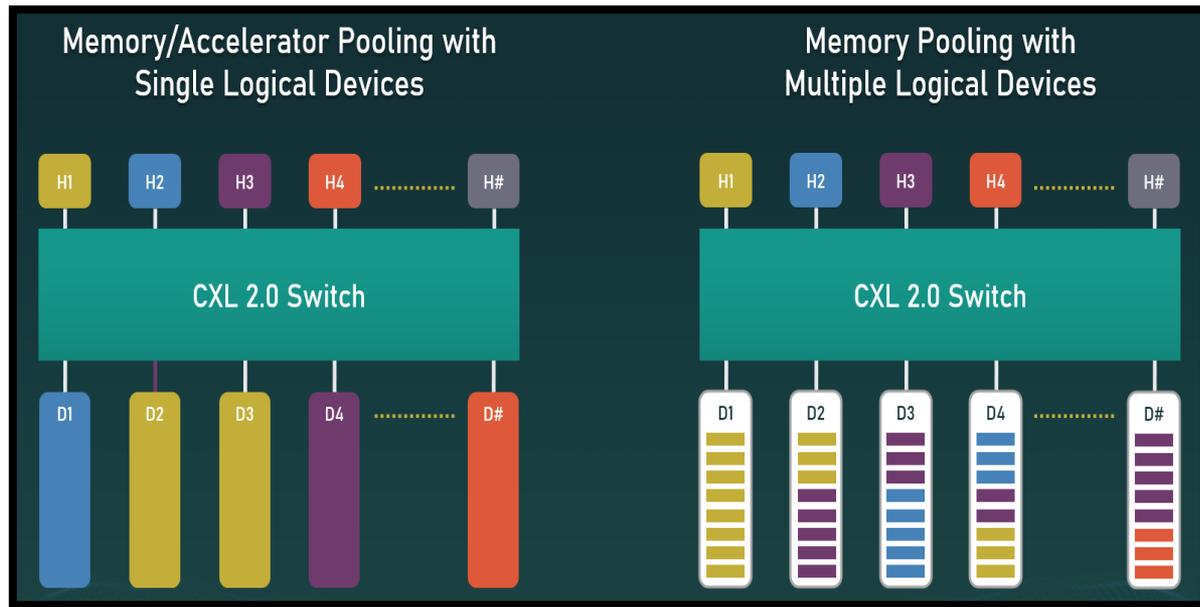# Applications for Memory Pooling / Sharing

- Xconn Tech's CXL switch to enable memory pooling and sharing

- Works with CXL 1.1 and CXL 2.0 server CPUs

Memory/Accelerator Pooling with Single Logical Devices

Memory Pooling with Multiple Logical Devices

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Thank you

Thank you!

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